REMARKS

Claims 1, 3-12 and 14-23 were examined in the application. Claims 1, 12 and 23 have been amended. Support for the Amendment is found in paragraph [0015] and FIGS. 1, 2 and 3. Applicant hereby requests further examination and reconsideration of the application in view of the following remarks.

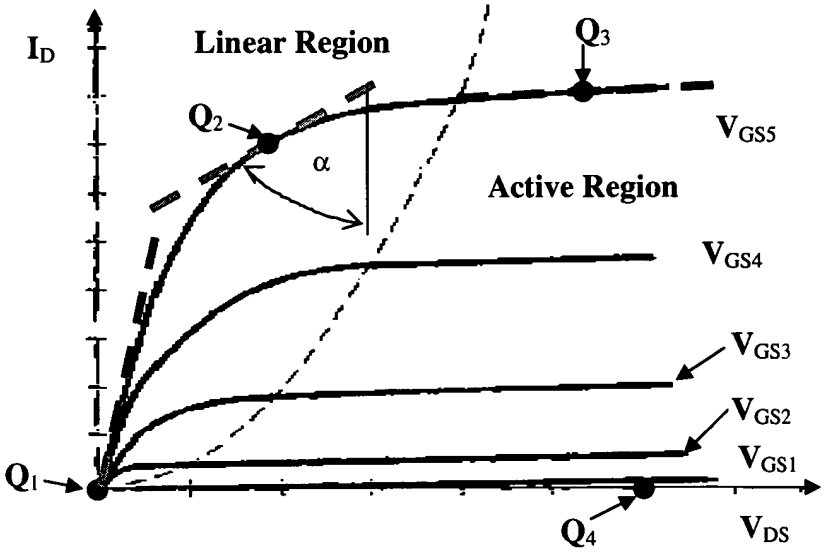
Claim Rejections – 35 U.S.C. §§ 102

The Patent Office rejected claims 1, 3-12 and 14-23 under 35 U.S.C. § 102(e) as being anticipated by Schultz et al., U.S. Patent No. 6,445,245 (Schultz). Applicant respectfully traverses the rejections of the remaining claims for at least the following reasons.

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *W.L. Gore & Assocs. v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). Further, "anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). Moreover, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Ryoka*, 180 U.S.P.Q. 580 (C.C.P.A. 1974). *See also In re Wilson*, 165 U.S.P.Q. 494 (C.C.P.A. 1970).

Claims 1, 12 and 23 now more particularly recite a plurality of N-channel devices each coupled *in series* with a discrete resister for providing a desired output impedance and a plurality of P-channel devices each coupled *in series* with a discrete resister for providing a desired output impedance. Thus, the present invention utilizes discrete resistors connected in series with the P/N channel devices. Nowhere does Schultz disclose, teach or suggest the use of discrete resisters connected *in series* with P/N channel devices which are arranged in parallel as claimed. Instead, Shultz reference discloses a system wherein the resistors are arranged *in parallel* with the P/N channel devices. The basic premises of this system can best be illustrated with one P and N channel device pair. Both the P and N

devices are turned on and the output node voltage is connected to a comparator. The comparator reference input is tied to a certain voltage such as ½VCC. If the output is at that potential (± the specified tolerance) this pair of devices is selected. If the output is above/below this range, more P or N channel devices are added until the desired level is achieved. This pair or a group of devices mirrors the comparator's input resistive voltage divider. For example, for ½VCC reference, both resistors are of equal value. Furthermore, their parallel combination $R_T = R_N \parallel R_P$ can be set to a desired value such as characteristic impedance Z_o of the transmission line.



MOS FET V/I Curves

The above figure shows the output V/I curves of a typical MOS FET transistor. The points Q_1, Q_2, Q_3 and Q_4 represent four extreme operating conditions of P or N channel devices mentioned in the previous paragraph. A tangential line, constructed at each operating point, has a unique angle α. The output resistance of the device at this operating point is equal to $R_o = \tan \alpha$. At the four extreme points Q_1, Q_2, Q_3 and Q_4, the output resistance R_o will vary from the lowest value for operating point Q_1 (i.e., the transistor operating in the linear region with $V_{DS} \approx 0$) to the largest R_o for the

point Q_3 (i.e., the transistor operating in the active region with $V_{DS} \approx V_{DD}$). At the operating point Q_4, the transistor is off and $R_o \approx \infty$. The variation of R_o is quite significant as a function of the drain-source voltage.

Consequently, the Shultz system is limited in that the termination will be $R_o = R_T = R_N \parallel R_P$ equal to the specified value only at one selected output voltage (i.e., at V_{out} = ½VCC). This is the operating point close to Q_2. Further, the output voltage of ½VCC occurs at one instance during the driver's output transition from low-to-high state and then in reverse. At the extreme ends (low and high) of the output voltage swing, Q_1, Q_3 and Q_4 will define the output resistance of the circuit. For purposes explanation, consider the low state. In this state, the N-channel is on with drain-source voltage $V_{DS} \approx 0$ operating in the linear region (operating point Q_1) and having the lowest R_o value. The P-channel operates in the off region (operating point Q_4) and has the highest value of R_o. The P-channel R_o is at least two orders of magnitude larger than the N-channel R_o. Thus, at this state, the equivalent output resistance is substantially different from the specified, desired R_T value of Z_o.

For operation of output driver, the low and high states are critical for the correct termination of the transmission line. After the completion of the output transition, reflected signals cause the overshoots and undershoots of the output waveform. In Schultz's system, there is a significant impedance mismatch between the driver's R_T in the low/high states and specified characteristic impedance of the transmission media. This mismatch can generate a new reflection, now traveling toward the receiver, and cause new signal integrity problems.

The addition of serial, discrete resistors R_{Ni} and R_{Pi} in accordance with the present invention *in series* with each device drain remedies the large differences between the output resistance values at the low and high output states, and the incidental R_o at ½VCC. In the example described, for the low state, the discrete resistor R_{Ni} compensates for the "loss" of parallel P-channel R_o. The N-channel device now has a serial discrete R_{Ni} to make up for the lowest R_o while functioning in the Q_1 operating point. The serial, discrete resistors act during the output transition as a negative feedback, linearizing the device

output resistance. The serial, discrete resistors of the present invention can be connected either to individual transistor devices or tied to a group of devices in order to generate an accurate termination for a range of typical characteristic impedances (e.g., 50Ω, 75Ω and 100Ω), or any other target in-between these values. Using the approach of the system described in Schultz, such an implementation would require a prohibitive silicon area.

Accordingly, it is respectfully submitted that 1, 3-12 and 14-23 are patentable over Schultz and the prior art in general. Withdrawal of the rejections under 35 U.S.C. § 102 is therefore respectfully requested.

CONCLUSION

The application is respectfully submitted to be in condition for allowance of all claims. Accordingly, notification to that effect is earnestly solicited.

Respectfully submitted,
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